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CORDIC-based GMSK systems: a review of modulation architecture, digital implementation, and hardware optimization

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ABSTRACT

Gaussian minimum shift keying (GMSK) is a continuous-phase digital modulation technique valued for its constant-envelope property and compact spectral occupancy. Its implementation in digital communication equipment requires accurate Gaussian pulse shaping, phase accumulation, and carrier generation, while maintaining low hardware complexity and power consumption. The coordinate rotation digital computer (CORDIC) algorithm offers an attractive computational approach because it generates trigonometric functions and performs vector rotations using shift-and-add operations rather than conventional multipliers. This review examines CORDIC-based GMSK systems, focusing on transmitter and receiver architectures, fixed-point computation, pipelined processing, and field-programmable gate array implementation. It discusses published designs that integrate CORDIC with frequency modulation and in-phase/quadrature signal generation, alongside developments in GMSK demodulation and CORDIC hardware architectures. The analysis highlights the trade-offs among numerical accuracy, processing latency, logic utilization, throughput, and power consumption. It also identifies challenges associated with Gaussian-filter realization, phase quantization, finite word length, and receiver synchronization. The review concludes by outlining research directions involving adaptive precision, resource sharing, low-power architectures, and integrated digital baseband implementation.

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1. INTRODUCTION

Digital communication systems require modulation techniques that use available spectrum efficiently while maintaining reliable data transmission. Gaussian minimum shift keying (GMSK) is an important continuous-phase modulation technique because it combines minimum frequency separation with Gaussian premodulation filtering. Its constant-envelope characteristic makes it suitable for nonlinear power amplifiers, while its reduced spectral sidelobes help limit adjacent-channel interference. These properties have supported its use in mobile radio and other bandwidth-constrained communication systems [1]–[4].

Despite these advantages, implementing GMSK digitally requires careful coordination of filtering, phase generation, and signal conversion. A conventional implementation may use lookup tables, multipliers, numerical oscillators, and additional arithmetic units to generate the required modulation waveform. Such structures can increase hardware utilization and complicate implementation on resource-constrained field-programmable gate array (FPGA) platforms. Therefore, a computational architecture that reduces arithmetic complexity without sacrificing waveform accuracy is valuable for practical GMSK systems.

The coordinate rotation digital computer (CORDIC) algorithm provides an alternative for generating trigonometric functions and performing coordinate rotations through iterative shift-and-add operations. Its multiplier-free structure makes it attractive for digital signal processing and communication hardware [5], [6]. Recent GMSK implementations have combined CORDIC with digital frequency synthesis to generate in-

phase and quadrature components and perform frequency modulation [7], [8]. This review evaluates these architectures and related developments, identifies their technical limitations, and discusses opportunities for more efficient GMSK hardware.

2. GMSK MODULATION FUNDAMENTALS

GMSK is derived from minimum shift keying, with a Gaussian low-pass filter applied to the input data before frequency modulation. The filter smooths the transitions of the baseband waveform and reduces the spectral sidelobes associated with abrupt signal changes. Its bandwidth-time product, commonly denoted by BT, determines the relationship between spectral compactness and intersymbol interference. A smaller BT generally reduces occupied bandwidth but increases the memory effect that must be considered in receiver design [1]-[3].

The GMSK transmitter typically consists of a binary data encoder, Gaussian filter, phase-generation stage, and carrier-generation circuit. The filtered data controls the instantaneous frequency deviation, while phase integration ensures continuous phase transitions between successive symbols. The resulting signal maintains an approximately constant envelope, which is beneficial for power-efficient radio-frequency amplification. However, the digital implementation must preserve phase continuity and sufficiently accurate waveform shaping to avoid spectral degradation [1], [2].

Receiver design introduces additional challenges because the transmitted phase information must be recovered in the presence of noise, frequency offset, and timing uncertainty. Coherent detection can provide strong error-rate performance but requires carrier and timing synchronization. Differential and non-coherent detection methods can reduce synchronization complexity, although their performance depends on the detection structure and channel conditions [3], [9]–[11]. Consequently, a complete GMSK implementation should consider transmitter waveform generation and receiver synchronization as interconnected design problems.

3. CORDIC ALGORITHM AND ITS ROLE IN GMSK

CORDIC is an iterative numerical method originally developed for efficient computation of trigonometric functions and coordinate transformations. Its main advantage is that many operations can be implemented using additions, subtractions, and binary shifts. This characteristic reduces dependence on general-purpose multipliers and can simplify hardware design in fixed-point digital systems. The algorithm has subsequently been developed into several architectural forms for signal processing, communication, and embedded applications [5], [6].

In a GMSK transmitter, CORDIC can be used to generate sine and cosine values from a digital phase representation. These values provide the in-phase and quadrature components required for carrier synthesis and modulation. The phase input is derived from the accumulated frequency-control signal, which is influenced by the Gaussian-filtered data. This arrangement allows a digital implementation to generate the modulated waveform without requiring a large trigonometric lookup table.

The suitability of CORDIC depends on its architecture and numerical configuration. Iterative structures reuse arithmetic units and reduce hardware resources, but their output latency increases with the number of iterations. Pipelined structures provide higher throughput by assigning successive CORDIC stages to separate processing elements, although they require more registers and logic resources. Fixed-point word length, iteration count, scaling compensation, and quadrant mapping must therefore be selected according to the required waveform accuracy and hardware constraints [5], [6], [12]–[17].

4. ARCHITECTURE OF CORDIC-BASED GMSK SYSTEMS

A representative CORDIC-based GMSK transmitter begins with binary input data and an encoding stage that produces a suitable non-return-to-zero sequence. The data then passes through a Gaussian filter to control the frequency-transition profile. A digital integration stage converts the filtered frequency-control sequence into a continuous phase trajectory. Finally, CORDIC generates the corresponding trigonometric components for the modulated carrier.

Kajur and Prasad presented an FPGA-oriented GMSK architecture using pipelined CORDIC and digital frequency synthesis [7]. Their system includes data encoding, Gaussian filtering, frequency modulation, and receiver processing, with CORDIC used in the modulation and demodulation chain. A related study by the same authors investigated an optimized CORDIC-based GMSK architecture using quadrant mapping and pipelining to improve implementation efficiency [8]. These works provide direct evidence that CORDIC can be integrated into practical GMSK hardware rather than being limited to isolated numerical-function generation.

A further implementation study describes GMSK hardware realization using a pipelined CORDIC module on FPGA [9]. This approach emphasizes the use of CORDIC for in-phase and quadrature signal generation, together with a digital frequency synthesizer. The architecture demonstrates the importance of coordinating modulation, carrier generation, and receiver processing within a single digital design. Nevertheless, implementation results should be interpreted in relation to the specific FPGA device, numerical precision, and evaluation methodology used in each study.

Receiver architecture requires additional functions that are not necessarily provided by the transmitter CORDIC block. These functions may include frequency recovery, timing recovery, demodulation, filtering, and data reconstruction. Qiu *et al*. [10] proposed a low-power digital GMSK baseband receiver for sub-GHz applications, integrating carrier recovery, timing recovery, and demodulation in a synthesizable circuit. Although this design is not itself a CORDIC-based receiver, it provides a useful reference for evaluating the system-level requirements that a practical CORDIC-based GMSK architecture must satisfy.

5. HARDWARE OPTIMIZATION AND IMPLEMENTATION TRADE-OFFS

The choice between iterative and pipelined CORDIC is a central architectural decision. An iterative design shares arithmetic resources across successive micro-rotations, making it attractive when field-programmable gate array area and power are more important than maximum throughput. A pipelined design can process successive input samples continuously after the pipeline is filled, making it suitable for high-data-rate applications. However, its larger register count and replicated arithmetic stages may increase area and switching power [5], [6], [12], [18]–[20].

Numerical precision is another important factor because finite word length affects the accuracy of the generated phase and carrier components. Insufficient precision can introduce phase error, amplitude deviation, and spectral distortion in the modulated output. Increasing the number of CORDIC iterations can improve numerical accuracy, but it may also increase latency and hardware requirements. A practical design should therefore evaluate the relationship between word length, iteration count, error vector magnitude, spectral characteristics, and bit-error rate rather than optimizing one metric independently [13]-[15], [17], [21].

Table 1 summarizes representative research relevant to CORDIC-based GMSK design and its supporting technologies. The table separates direct GMSK-CORDIC implementations from studies that contribute to GMSK receiver design or CORDIC architecture. This distinction is necessary because the latter provide supporting methods but do not independently demonstrate a complete CORDIC-based GMSK system. The comparison also highlights the need for more consistent hardware evaluation across published implementations.

Table 1. Representative research relevant to CORDIC-based GMSK systems

Reference	Main contribution	Relevance to GMSK-CORDIC design
Kajur and Prasad [7]	Pipelined CORDIC GMSK system on FPGA	Direct transmitter and receiver architecture
Kajur and Prasad [8]	Optimized CORDIC-based GMSK implementation	Quadrant mapping and hardware optimization
Kajur and Prasad [9]	FPGA realization using pipelined CORDIC	Digital frequency synthesis and I/Q generation
Qiu *et al*. [10]	Low-power GMSK digital baseband receiver	Receiver synchronization and demodulation
Lakshmi and Dhar [12]	CORDIC architecture survey	Architectural design principles
Meher *et al*. [13]	Review of CORDIC algorithms and architectures	Accuracy, latency, and hardware trade-offs
Lyu *et al*. [14]	Optimized CORDIC hardware	Resource sharing and critical-path reduction
Salehi *et al*. [15]	Low-latency CORDIC implementation	Reduced iteration latency
Mohamed *et al*. [21]	Reconfigurable CORDIC implementation	Flexible hardware configuration

Table 1 shows that direct GMSK-CORDIC research has established the feasibility of integrating pipelined CORDIC with digital modulation and FPGA implementation. Related CORDIC studies provide additional techniques for improving latency, hardware utilization, and numerical accuracy [12]-[15], [21]. Meanwhile, the GMSK receiver literature demonstrates that carrier and timing synchronization remain important even when the transmitter waveform is generated efficiently [10]. These findings indicate that optimization should address the complete communication chain rather than the CORDIC block alone.

6. PERFORMANCE EVALUATION AND RESEARCH CHALLENGES

A meaningful assessment of CORDIC-based GMSK systems should combine communication-level and hardware-level performance indicators. Communication metrics include bit-error rate, occupied bandwidth, spectral sidelobe level, and waveform quality. Hardware metrics include logic utilization, register count, maximum operating frequency, latency, throughput, and power consumption. Evaluating both groups

is necessary because a design with low FPGA area may still produce unacceptable communication performance.

One important challenge is the interaction between Gaussian filtering and finite-precision phase generation. Quantization in the filter coefficients and CORDIC datapath can affect the phase trajectory and therefore the transmitted spectrum. The receiver may also experience performance degradation if synchronization errors or channel impairments are not considered during evaluation. Future studies should investigate these effects together using realistic channel models and hardware measurements.

Another challenge concerns the fair comparison of CORDIC architectures. Published implementations may use different FPGA families, clock constraints, word lengths, Gaussian-filter parameters, and measurement procedures. Direct comparison of reported area or speed values can therefore be misleading when the underlying design conditions are not equivalent. A reproducible evaluation framework should specify the modulation parameters, numerical format, channel conditions, synthesis settings, and measurement methods.

7. FUTURE RESEARCH DIRECTIONS

Future research should investigate adaptive CORDIC architectures that adjust iteration count and numerical precision according to communication requirements. Such designs could reduce unnecessary arithmetic activity when lower precision is sufficient while retaining higher accuracy for demanding operating conditions. Resource sharing between carrier generation and other digital baseband operations may also reduce hardware overhead. These approaches should be evaluated for their effects on throughput, latency, and power consumption.

Another promising direction is the integration of CORDIC-based modulation with a complete low-power digital receiver. This requires coordinated optimization of Gaussian filtering, phase generation, carrier recovery, timing recovery, and demodulation. FPGA and ASIC implementations should be compared using consistent communication and hardware metrics. Experimental testing under noise, frequency offset, and timing uncertainty would provide stronger evidence of practical system performance.

8. CONCLUSION

CORDIC-based GMSK systems offer a practical approach to digital modulation by combining the spectral advantages of GMSK with the multiplier-reduced computational structure of CORDIC. Published FPGA implementations demonstrate that CORDIC can support phase generation, frequency modulation, and in-phase/quadrature signal generation in GMSK architectures. Related studies also show that pipelining, quadrant mapping, and optimized numerical configurations can improve hardware efficiency. However, the overall performance remains dependent on Gaussian-filter accuracy, finite word length, synchronization quality, and the selected CORDIC architecture. Further progress requires system-level optimization rather than isolated improvements to the CORDIC processor. Future implementations should jointly assess spectral performance, bit-error rate, hardware resources, latency, and power consumption under consistent test conditions. Adaptive precision, resource sharing, and integrated transmitter–receiver architectures are promising research directions. These developments can strengthen the suitability of CORDIC-based GMSK for compact, low-power, and configurable digital communication platforms.

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