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Placement of solid-state circuit breaker at microgrid for different types of faults

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ABSTRACT

A direct current (DC) microgrid is a localized electrical network that uses DC for power distribution and integrates renewable energy sources, such as solar panels and batteries, with electronic loads, reducing conversion losses. DC microgrids improve reliability, reduce transmission losses, and support off-grid and remote applications. Solid-state circuit breakers (SSCBs) enhance protection and control by rapidly interrupting current, minimizing arc formation, and improving system resilience. Fast fault isolation is essential to maintaining DC microgrid stability and efficiency. Distributed energy resources (DERs) and loads are connected to the DC mains through power electronic converters. The proposed system consists of three DC feeders, each supplying three loads through individual breakers. A rectifier converts alternating current (AC) power from the main grid into DC when DER power is unavailable, while DERs and batteries directly supply DC power. This study analyzes different microgrid fault conditions and applies intentional islanding to improve the reliability and resilience of DERs in a low-voltage direct current (LVDC) system. The proposed system is modeled and analyzed using MATLAB/Simulink.

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1. INTRODUCTION

Over the past century, the structure of electrical power systems has undergone significant change, moving from centralized generation to more distributed and decentralized models. This evolution has led to the development of new technologies, one of which is the direct current (DC) microgrid—an energy system that uses DC to integrate distributed energy resources (DERs), storage, and DC loads more efficiently. With increasing focus on environmental sustainability and energy efficiency, DC microgrids have gained importance, especially with the rapid adoption of renewable energy sources such as solar photovoltaics (PV) and wind power. However, this progress also introduces new challenges, particularly in fault protection and the quick isolation of faults in these systems. This work examines the development, benefits, and protection strategies of DC microgrids, highlighting their growing role in modern energy distribution.

Conventional power systems have historically relied on centralized alternating current (AC) networks. This model is now evolving as more users turn to local energy generation, driven by factors such as: the growing use of renewable energy technologies, the increasing number of electric vehicles (EVs) and DC-powered devices, and the demand for improved energy resilience amid grid fluctuations.

DC microgrids stand out in this transition, largely because many renewable energy sources generate DC power inherently, eliminating unnecessary conversion losses that typically occur when switching from AC to DC and back. The integration of distributed generation (DG) into DC microgrids presents several challenges, particularly in maintaining stability and ensuring effective fault protection. During normal operation, DG units' function in grid-connected mode, but during grid interruptions, they must transition to islanded mode and independently supply local loads. To detect islanding scenarios, various techniques have been proposed. Al-Wadie *et al.* [1] introduced a fast angle estimation method, while Lee *et al.* [2] applied time-domain analysis of active and reactive power. Wang *et al.* [3] explored reactive power variation in the frequency domain, and Li *et al.* [4] developed an impedance voltage divider-based detection approach. However, load control within islanded mode was not addressed in these studies. Kumar and Laxmi [5] contributed by developing an islanding detection scheme with integrated load control, enabling isolation of faulty loads while maintaining healthy DER connections.

Protection of DC microgrids further requires fast and reliable fault isolation, as high fault currents can quickly damage sensitive equipment. Rapid disconnection of faulted sections is therefore critical. Byeon *et al.* [6] work on fault current characteristics in AC and DC systems has provided valuable insights for designing protection strategies. The researchers [7]–[9] proposed comprehensive protection schemes for hybrid AC/DC microgrids, addressing both AC and DC fault conditions. Additionally, solid-state circuit breakers (SSCBs) have emerged as an advanced solution for high-speed fault isolation. Eswaraiah and Laxmi [10] proposed a bidirectional SSCB with advanced current differential protection, enabling rapid fault interruption. Munasib and Balda [11] examined protection for low-voltage DC microgrids, highlighting the advantages of fast-acting SSCBs. Sun *et al.* [12] further improved SSCB control, enhancing system speed and coordination for reliable fault handling.

Despite the advancements within the DC microgrids, there is a lack of comprehensive methods for optimal SSCB placement in complex microgrids. Most studies focus on singular fault types; real systems must contend with a variety of scenarios like line-to-line, line-to-ground faults, and open circuit fault. The interaction between SSCBs and various DERs remains underexplored.

The main objective of this project is to develop and design a detailed DC microgrid model, incorporating three distribution feeders, each supplying power to three individual loads. The microgrid is energized through a combination of DERs, battery storage systems, and rectified AC power from the main utility grid. A core aspect of this work is to implement and simulate bidirectional SCCB, modeled based on the design proposed by Eswaraiah and Laxmi [13]. This SSCB operates using a current differential protection strategy, enabling reliable and rapid fault isolation within DC bus.

2. BLOCK DIAGRAM

Figure 1 shown is a low-voltage direct current (LVDC) microgrid was modeled using. The system comprises of three feeders with each feeder is connected to three individual DC loads, totaling nine loads. The power sources are solar PV array (DC output), battery system (48 V DC), main AC grid connected via AC-DC rectifier for backup supply. Power electronic converters are used for source integration and voltage regulation. Each load is interfaced through individual switches to allow selective isolation during fault conditions.

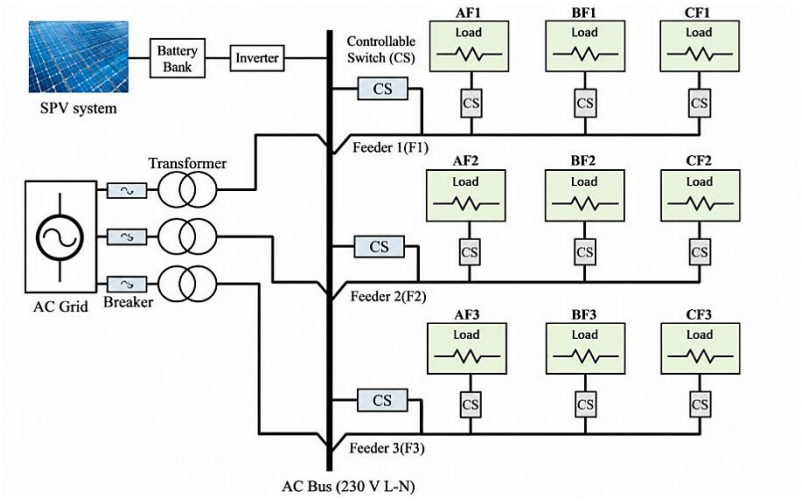


Figure 1. LVDC distribution system with DC line protection circuit

3. PROTECTION STRATEGIES

There is a protection strategy that is to protect the system when a DC line fault occurs using the. The protection scheme proposed by Eswaraiah and Laxmi [13] in their paper "Protection of DC line with distributed generator in intentional islanding mode" combines three coordinated strategies to detect and isolate DC faults in microgrids.

- Voltage drop detection: a fault is assumed if the voltage across the DC line drops by 10 V or more, indicating abnormal system behavior.
- Differential current strategy (KCL violation): the system checks for imbalance in incoming and outgoing current. If the differential current (Id) exceeds 0.01 A, a fault is declared.

$$Id = | Iin - Iout | \geq 0.01 \text{ A}.$$

- Backup protection (time delay logic).

If a high current persists beyond a preset time, the breaker trips as a fallback protection. These strategies are implemented in MATLAB/Simulink using a logic-based control. A [CB] signal controls the breaker state—remaining high during normal operation and going low during a fault to isolate the circuit. This scheme ensures fast, selective, and reliable protection, particularly useful in systems with DERs and intentional islanding.

Figure 2 shown is algorithm that starts by continuously monitoring the current flowing through the DC line and the voltage level at the distributed generator. It then evaluates multiple logical conditions, triggering the circuit breaker only when a confirmed fault condition is detected. The flowchart used for this logic implementation is adapted from the method described in [13]. Although the base protection scheme can detect and isolate faults, it does not suppress the initial surge of fault current or prevent the occurrence of reverse current after clearing the fault. To mitigate these limitations, a SSCB is integrated with the protection scheme. This enhancement enables faster fault interruption, significantly limits high fault currents and supports smoother system recovery without introducing negative current effects.

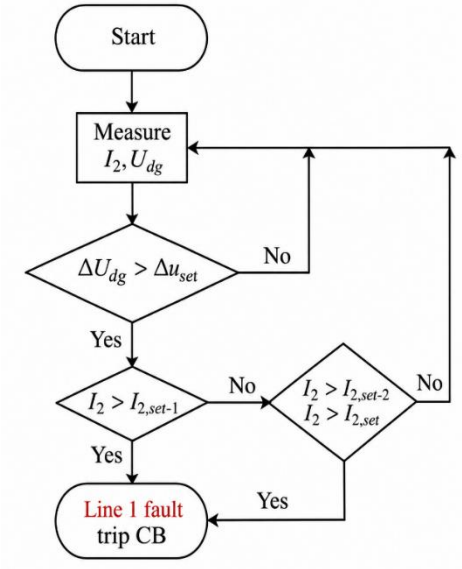


Figure 2. Control algorithm

3.1. Implementation of solid-state circuit breaker

The SSCB is integrated into the DC microgrid to enhance fault isolation speed and control transient energy during faults. It is installed in series with the DC bus and operates based on a current differential protection method. The SSCB can interrupt fault currents in both directions and allows automatic reclosing, making it suitable for modern LVDC applications, as described in [10].

Figure 3 SSCB includes key components for reliable and fast fault handling. Two insulated-gate bipolar transistors (IGBTs) (Q1 and Q2) are connected in reverse series to support bidirectional current flow under normal conditions. In parallel, silicon-controlled rectifiers (SCRs) (T1 and T2) are placed in reverse parallel to provide a bypass path for fault current. A blocking capacitor (C) stores the fault energy, protecting

downstream equipment. Once the fault is cleared, a triode for alternating current (TRIAC) and a discharge resistor (Re) release the energy from the capacitor in a controlled manner. This configuration enables rapid fault interruption and supports quick system recovery.

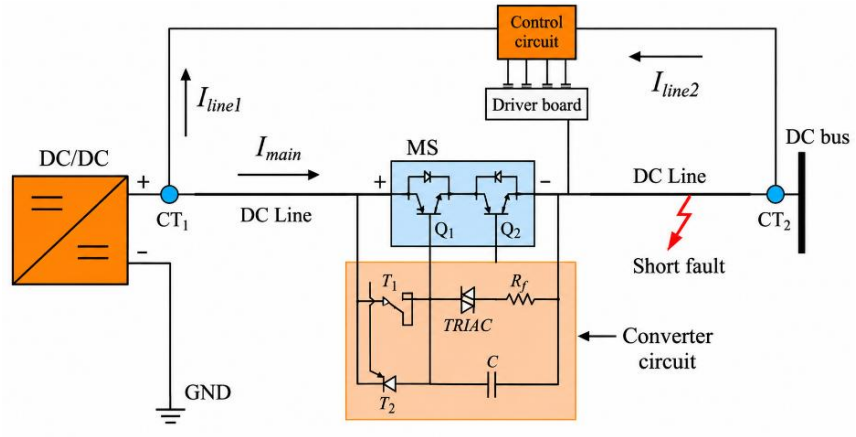


Figure 3. SSCB

The SSCB operates in four main stages, illustrated in the corresponding Figure 4. In normal mode, the IGBTs carry the rated current with low conduction losses (Figure 4(a)). Once a fault is detected, the system enters capacitor charging mode, routing current through the SCRs to charge the blocking capacitor (Figure 4(b)). When the current falls below the SCR holding threshold, the breaker transitions to fault-current blocking stage, isolating the faulty section (Figure 4(c)). After a brief delay, reclosing mode resumes normal operation by switching the IGBTs back ON Figure 4(d)).

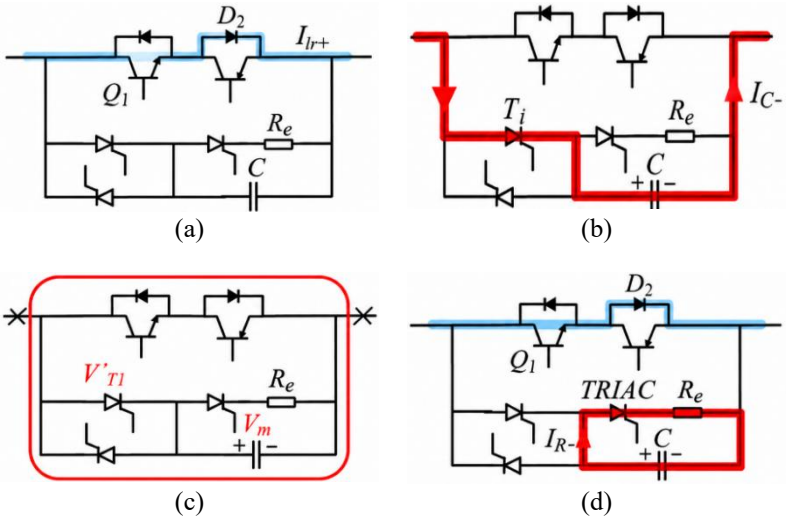


Figure 4. Current flow path of SCCB; (a) normal operating mode, (b) capacitor charging mode, (c) fault-current blocked mode, and (d) reclosing stage and dump energy releasing stage

4. SIMULATION RESULTS

4.1. System design

The system includes an 11 kV substation connected to a three-phase transformer through a medium-voltage breaker. The voltage is reduced to 230 V (L-N) and 440 V (line-to-line), then converted to DC using an AC/DC rectifier. The DC bus receives power from both the rectified grid and a PV array. In the event of a

grid outage, the PV array continues supplying critical DC loads, maintaining continuous operation. This model builds on the setup described in the previous study, where a line-to-line fault near the PV terminal was examined using voltage and current-based protection. In this study, a SSCB is incorporated and additional fault cases—line-to-line, line-to-ground, open-circuit, and high-impedance faults (HIFs)—are introduced to further assess system performance under different fault conditions.

4.2. Results and discussion

4.2.1. Line-to-line fault

As depicted in Figure 5, the system response during a line-to-line fault (0.2–0.3 s) improves notably with the inclusion of the SSCB. The peak fault current is reduced from 4020 A to 2822 A and the negative current observed at 0.3 s is entirely suppressed (0 A instead of –1024 A). This highlights the SSCB's capability to effectively control fault current, eliminate reverse current, and aid in the smooth recovery of normal operation.

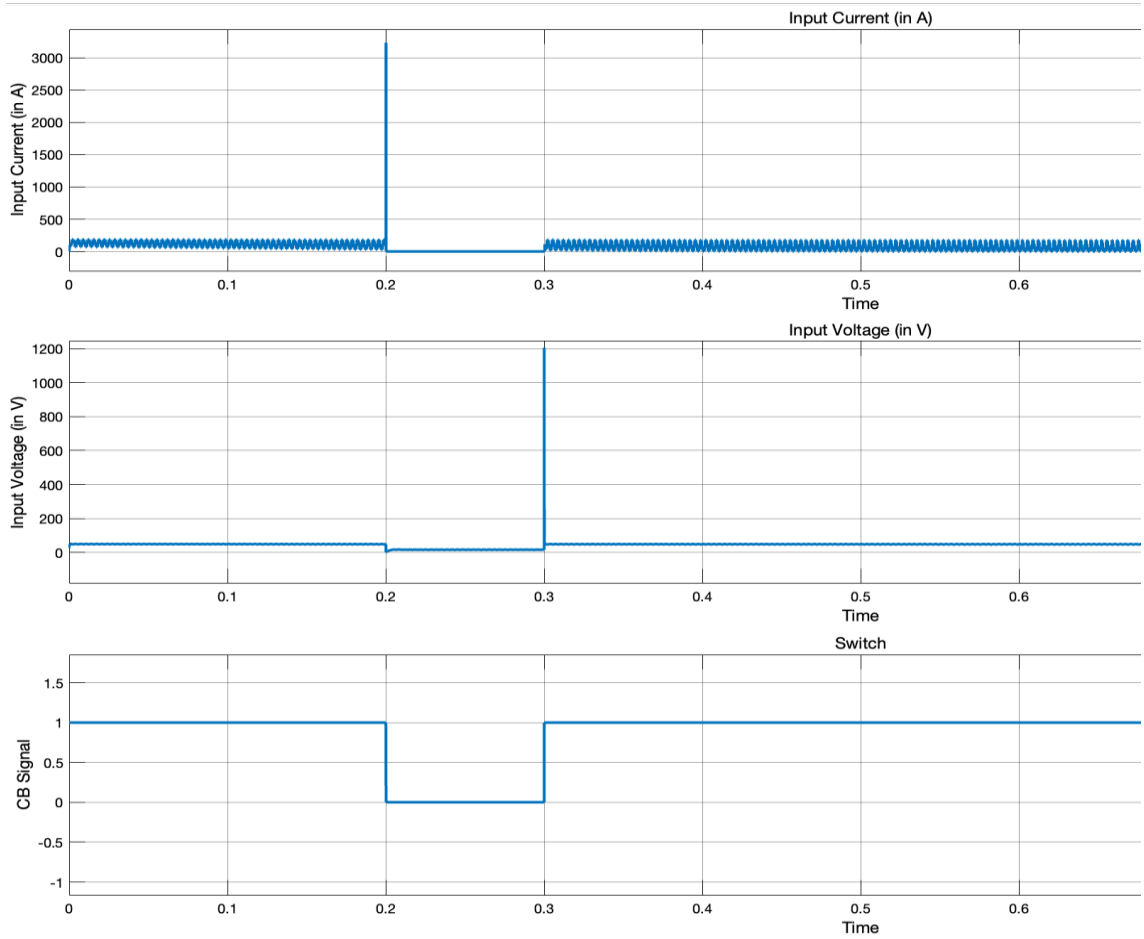


Figure 5. Waveforms of input current, voltage, and switch of line-to-line fault

Figure 6 shows bus voltage and current during a line-to-line fault. Initially, the voltage is steady at 48 V and current at 60–64 A. During the fault (around 0.2 s), voltage drops to 15–17 V and current to 20–22 A. At 0.3 s, a sharp transient occurs with voltage spiking to 1200 V and current peaking at 969 A, followed by system recovery.

Figure 7 illustrates the load voltage, current, and power profiles during the fault event. At 0.2 s, a sharp voltage drops to approximately 15 V is observed, along with a decrease in current below 10 A and power approaching zero. Following fault clearance at 0.3 s, voltage rises to nearly 96 V, current exceeds 60 A, and power surpasses 1800 W. The system then rapidly stabilizes to its normal operating state.

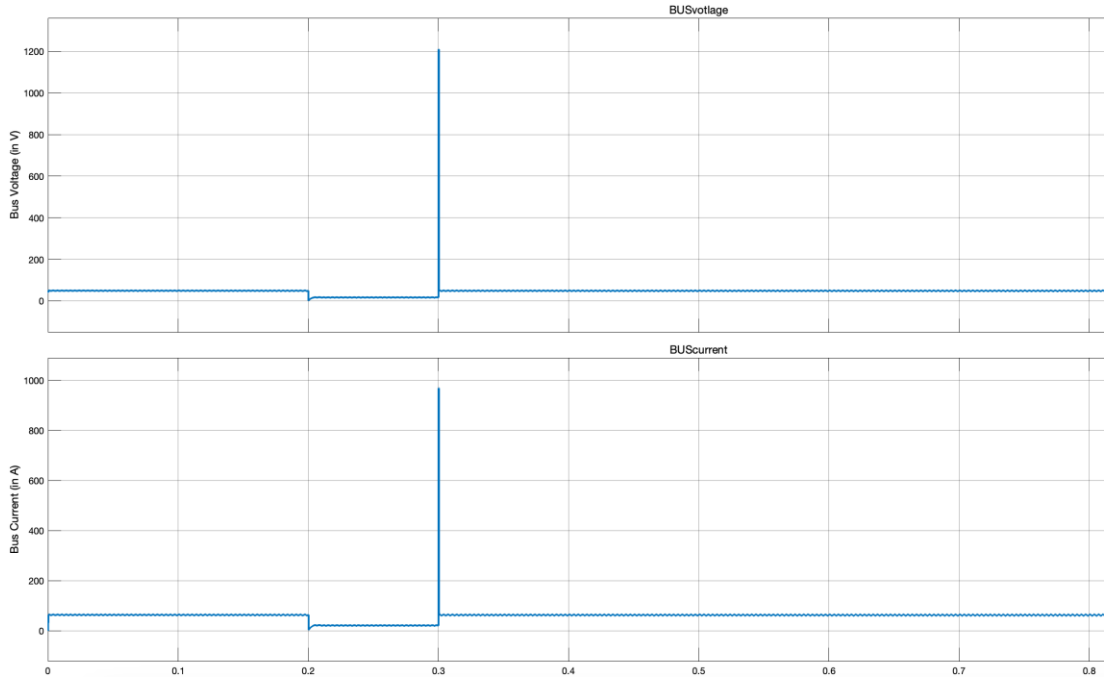


Figure 6. Waveforms of bus voltage and current during line-to-line fault

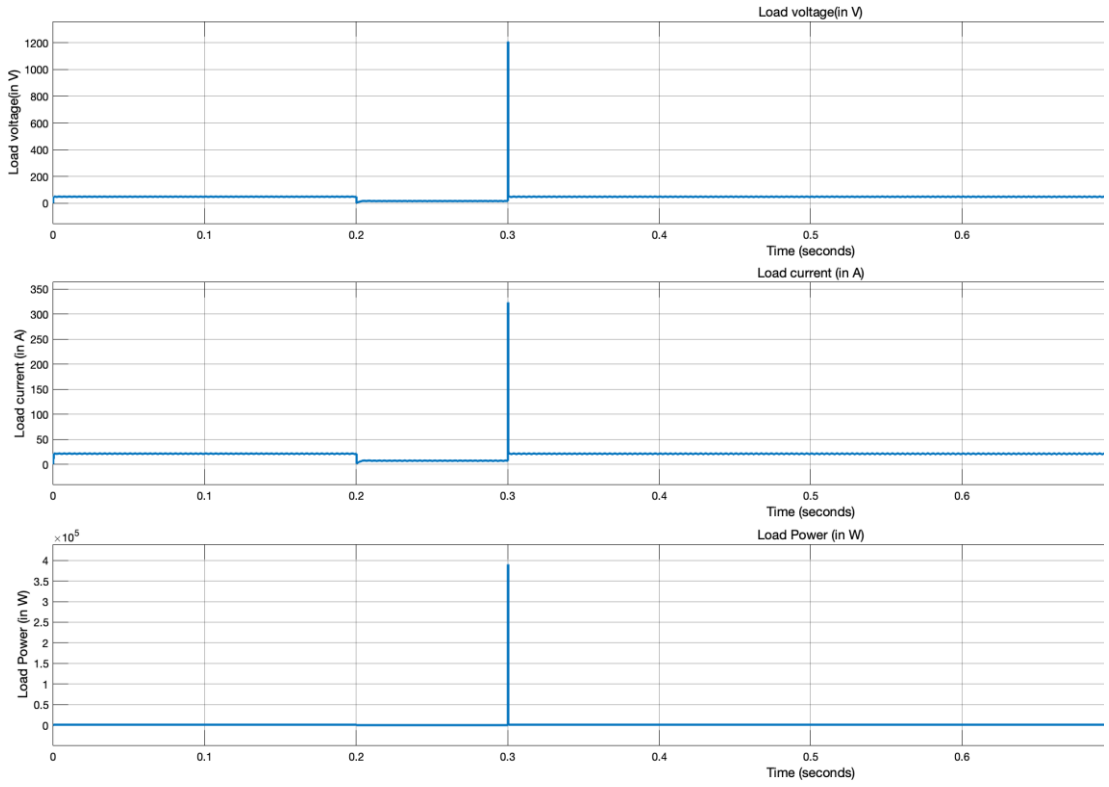


Figure 7. Waveforms of load voltage, current, and power during line-to-line fault

4.2.2. Line-to-ground fault

Figure 8 shows input current, voltage, and CB signal during a line-to-ground fault with SSCB and protection. At 0.2 s, current peaks at 1833 A and voltage drops to 25 V. The breaker triggers at 0.239 s, cutting

current to 0 A and restoring voltage. By 0.3 s, isolation is confirmed (283 V, 0 A). Normal conditions resume around 0.85 s, with no negative current observed, showing effective fault clearance.

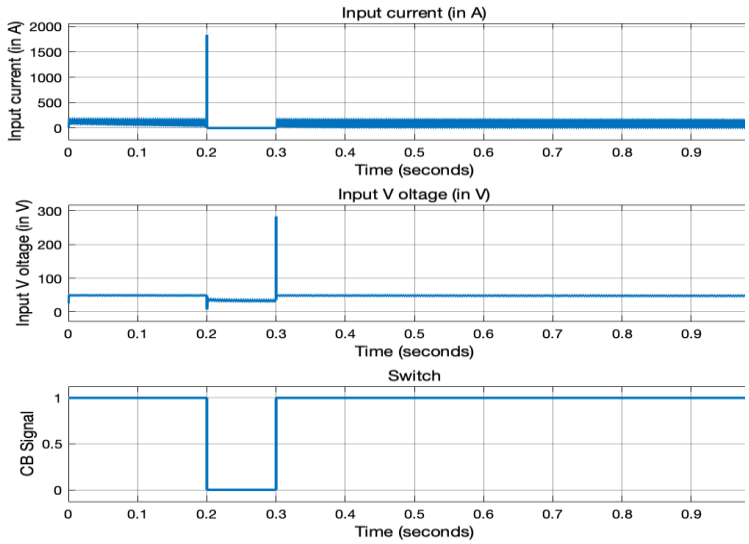


Figure 8. Waveforms of input current, voltage, and switch of line-to-ground fault

Figure 9 shows the bus voltage and current response during a line-to-ground fault. At 0.2 s, the fault causes the bus voltage to dip to around 25 V and the current to drop to roughly 40–50 A. By 0.3 s, a transient spike occurs, with voltage peaking at nearly 290 V and current reaching about 250 A. After the fault is cleared, both voltage and current stabilize, indicating effective system recovery.

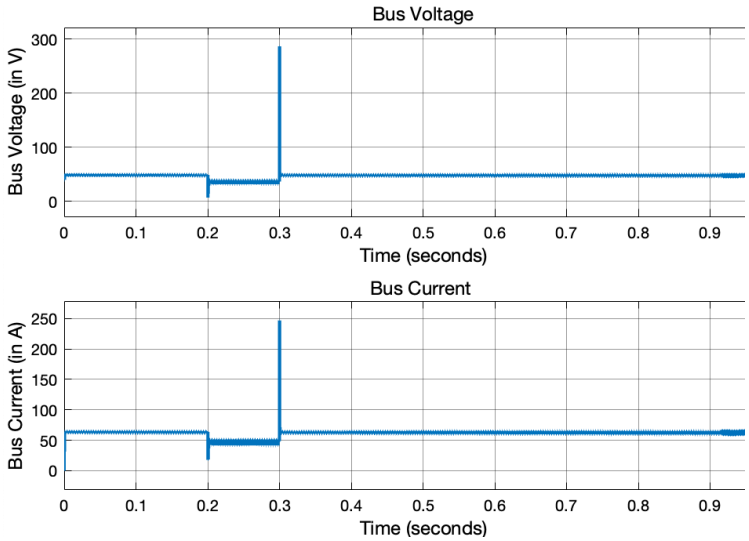


Figure 9 Waveforms of bus voltage and current during line-to-ground fault

Figure 10 illustrates output voltage, current, and power during an line-to-ground fault with SSCB and protection scheme. At 0.2 s, voltage and current drop to 7.2 V and 6.17 A. By 0.239 s, they recover to 39.38 V and 17.08 A. At 0.3 s, peak values of 286.4 V and 82.2 A are observed, delivering high power. The system stabilizes at 48.74 V and 21.11 A by 0.85 s.

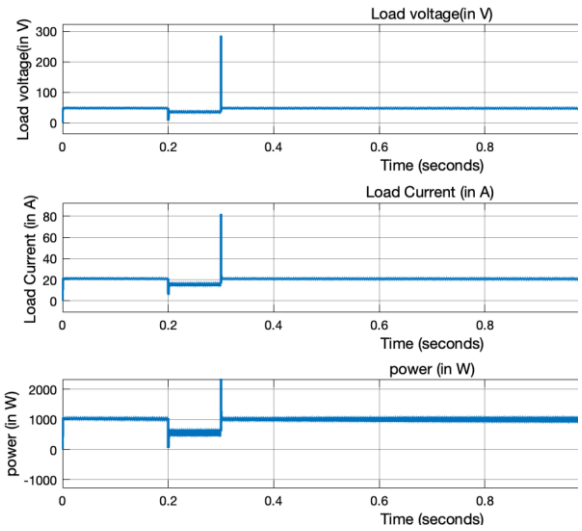


Figure 10. Waveforms of load voltage, current, and power during line-to-ground fault

4.2.3. Open circuit fault

Figure 11 shows the input current, voltage, and switch control during an open-circuit fault (line disconnection). The switch opens between 0.2 s and 0.3 s, cutting current flow and creating the fault. The current drops to zero, while voltage remains stable. The SSCB does not operate here, as open-circuit faults do not produce fault current to trigger its action.

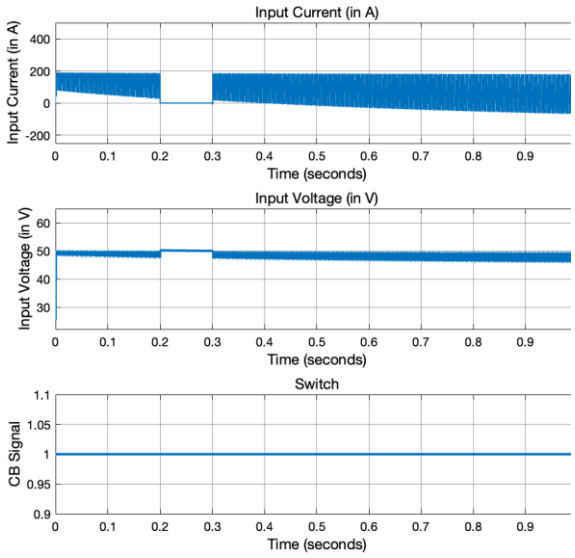


Figure 11. Waveforms of input current, voltage, and switch during open circuit fault

Figure 12 shows the bus voltage and current during an open-circuit fault. At 0.2 s, the fault causes a drop in voltage and current. The current decreases sharply due to circuit interruption, while voltage shows some fluctuations. By 0.3 s, the system begins to recover. Since no high fault current is present, the SSCB does not operate in this condition.

Figure 13 shows the output voltage, current, and power waveforms during an open-circuit fault. The disconnection between 0.2 s and 0.3 s causes a drop in voltage and power at the load. However, load current does not reach zero, as the AC grid continues supplying current via an alternate path. The voltage dip reflects the loss of PV contribution, while power remains due to grid support, ensuring system continuity during the fault.

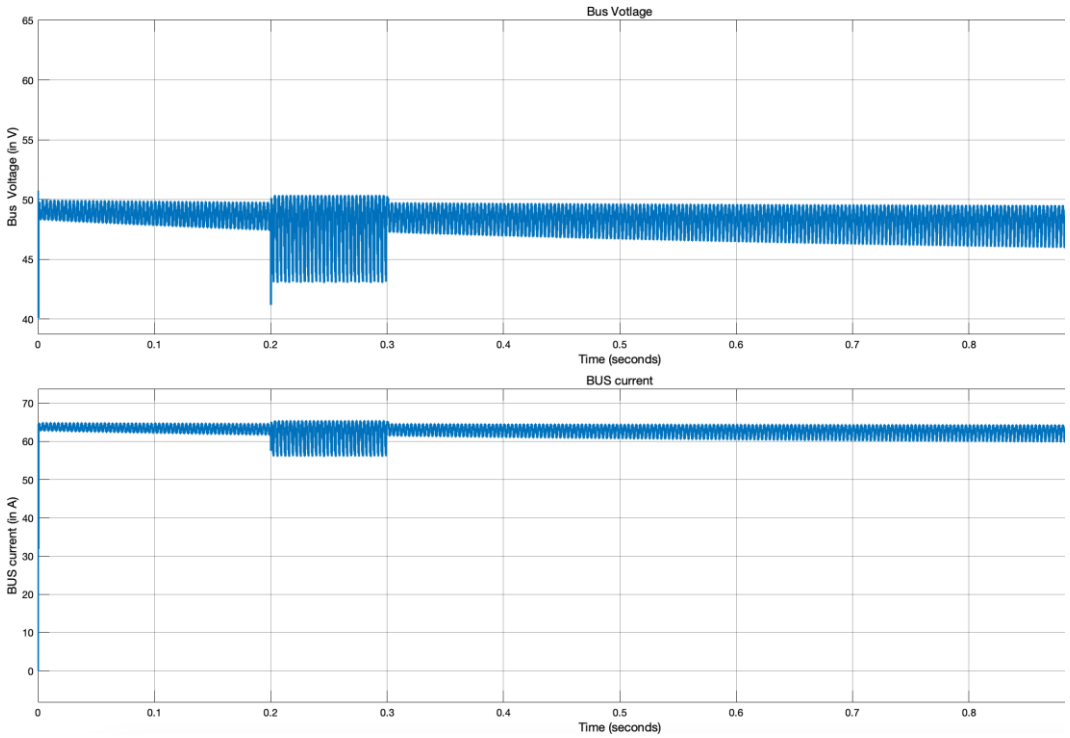


Figure 12. Waveforms of bus voltage and current during open circuit fault

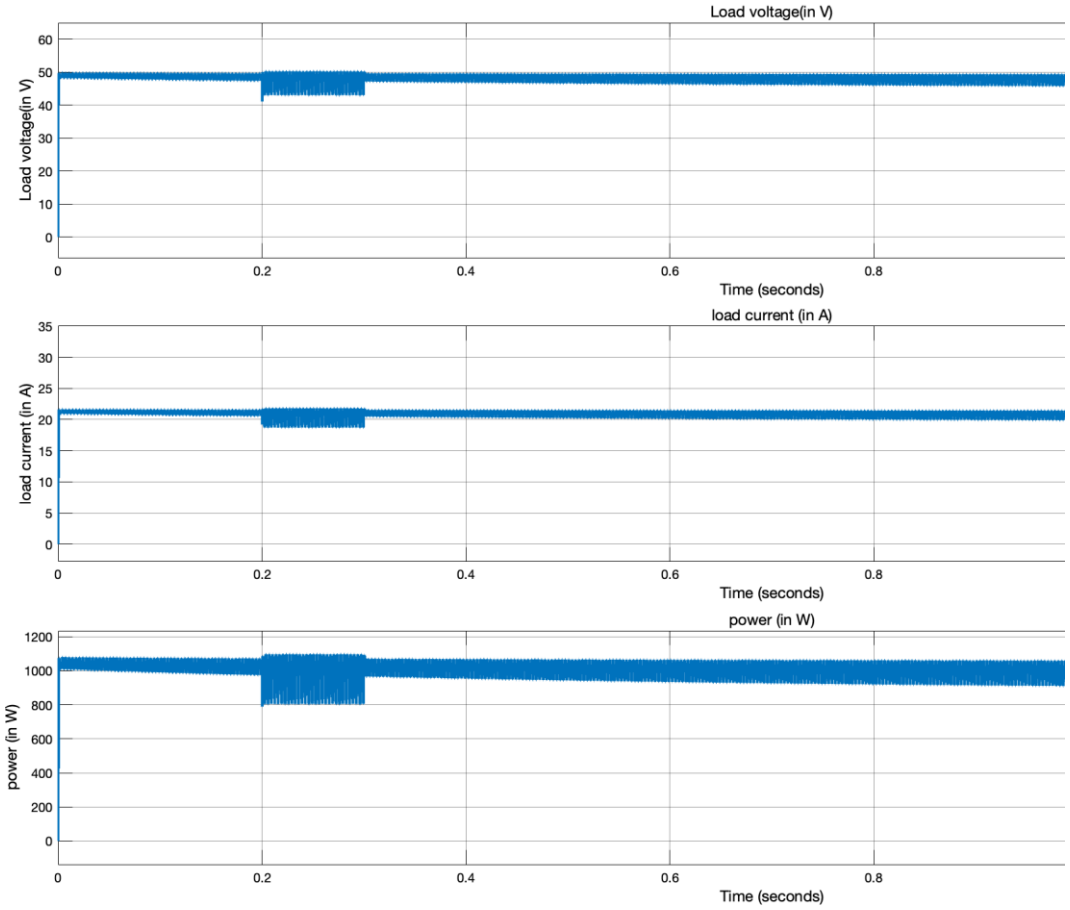


Figure 13. Waveforms of load voltage, current, and power during fault

4.2.4. High impedance fault

Figure 14 illustrates the system's behavior under a HIF introduced between 0.2 s and 0.3 s. The input current drops sharply to nearly zero during the fault, as the high resistance limits current flow instead of causing a surge. After 0.3 s, the current gradually recovers. The input voltage shows a transient spike at fault inception, then slightly reduced levels during the fault, with full recovery later. The switch signal stays high, indicating the fault was externally applied and not isolated by the switch. HIF cause subtle changes, making them harder to detect than direct shorts.

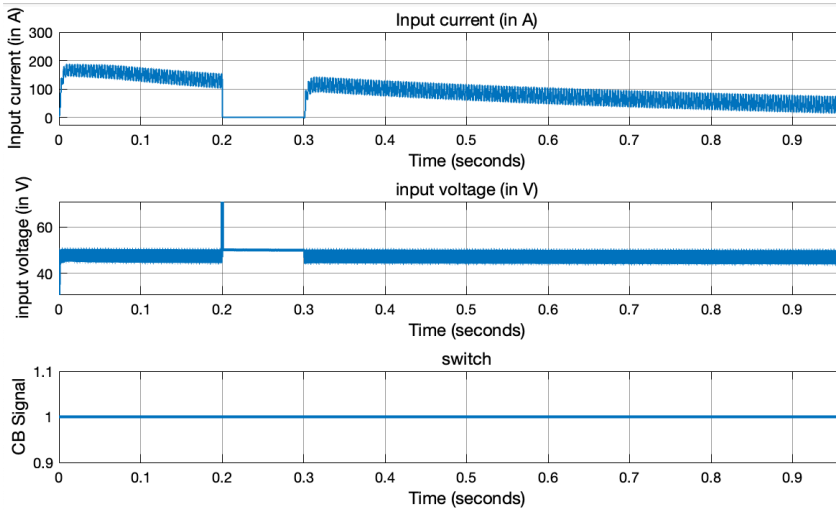


Figure 14. Waveforms of input current, voltage, and switch during HIF

The bus voltage and current waveforms during a HIF are shown in Figure 15. At the fault instant (around 0.2 s), both voltage and current exhibit a sudden dip, reflecting the impact of the fault path resistance, which limits current flow without creating a complete short. After the fault is cleared, both signals quickly return to normal. The system maintains overall stability, as the HIF causes subtle disturbances rather than severe disruptions.

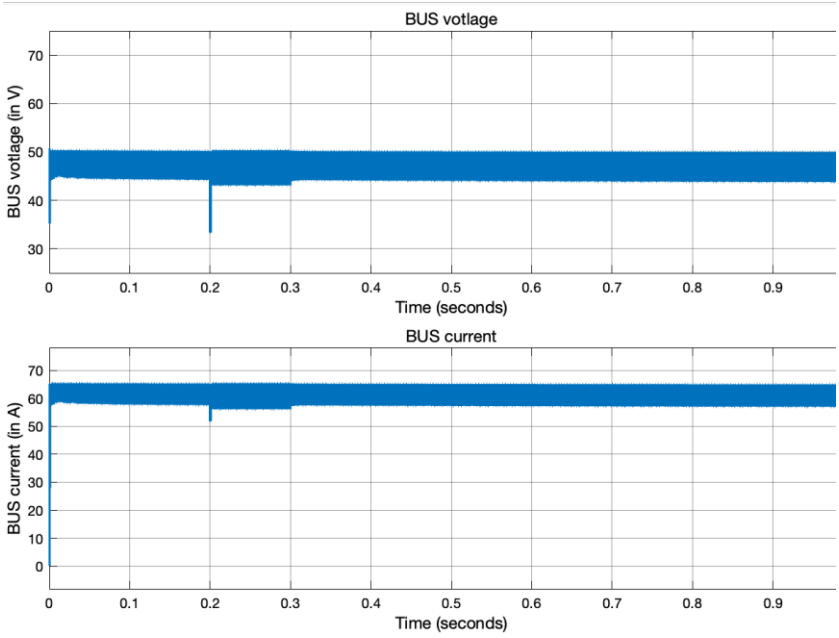


Figure 15. Waveforms of bus voltage and current during HIF

Figure 16 displays the load voltage, current, and power under a HIF. Due to the fault's high resistance, current flow to the load is restricted but not completely blocked. Consequently, the load current and power decrease between 0.2 s and 0.3 s, without falling to zero. The load voltage remains mostly stable, showing only slight disturbances. Unlike an open-circuit fault, some power continues to reach the load, allowing the system to operate at reduced capacity during the fault.

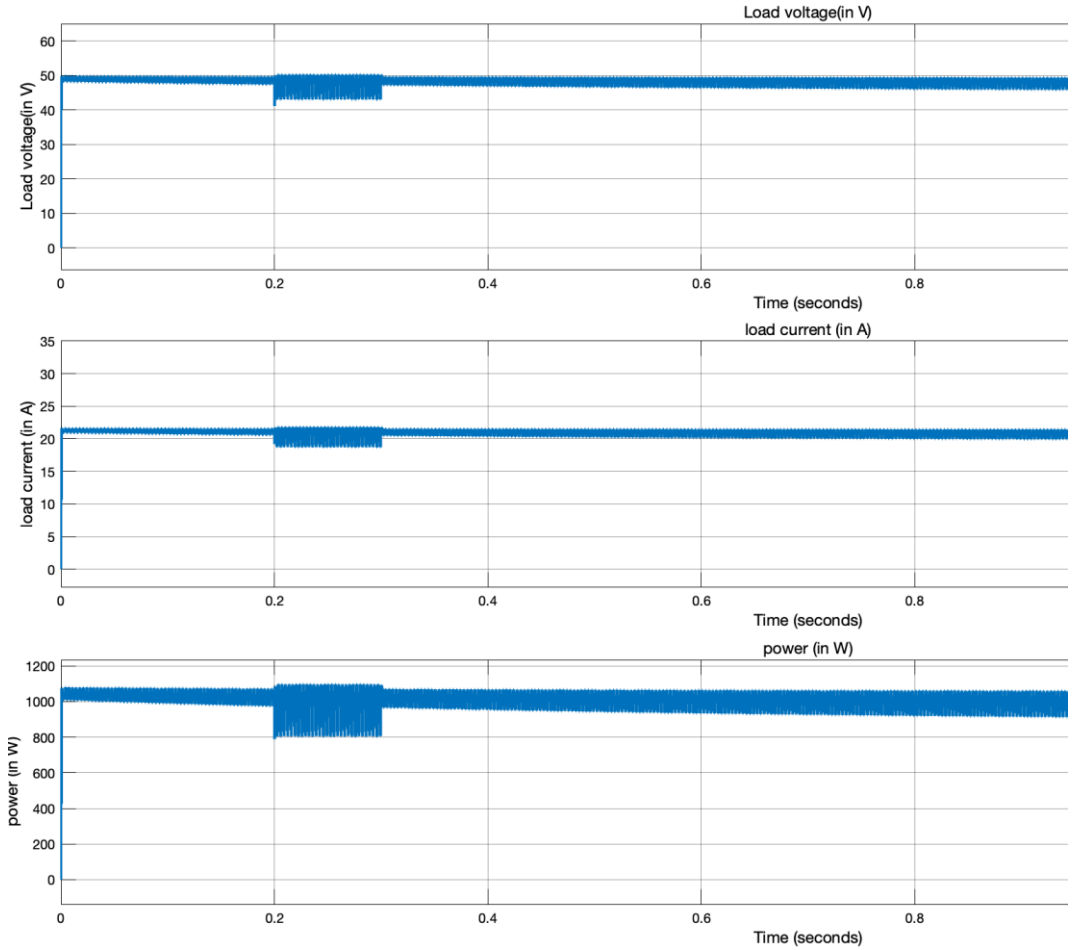


Figure 16. Waveforms of load voltage, current, and power during HIF

Table 1 presents the variation in fault current for different resistance values used to simulate HIF at the PV source side. As resistance increases, the fault current reduces sharply—from 22.75 A at 0.3 Ω to just 0.0281 A at 250 Ω. While lower resistance faults generate detectable currents, higher resistance faults result in very low currents, which are difficult for conventional protection devices to sense. This highlights the need for advanced protection schemes to accurately detect HIFs in DC microgrids.

Table 1. System response for varying fault resistance values

No.	Resistance (Ω)	Current (A)
1.	0.3	22.75
2.	0.5	14.56
3.	1	6.894
4.	10	0.7
5.	50	0.1402
6.	100	0.0707
7.	150	0.0468
8.	200	0.03512
9.	250	0.0281

5. CONCLUSION

The paper demonstrated an effective fault protection method for DC microgrids by combining a voltage-based and current-based logic scheme with a SSCB. Simulations of various fault types—line-to-line, line-to-ground, open-circuit, and high-impedance—showed that the SSCB quickly isolated short-circuit faults, reducing system stress. In open-circuit and HIFs, low current levels meant the SSCB remained inactive, as expected. This confirms the need for fault-specific protection strategies. The overall approach improved system safety and reliability, with results validated through MATLAB/Simulink.

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